Claims

1. Device comprising an array (1) of microsystems (2) which can be individually addressed by a control circuit (3), characterized in that the control circuit (3) and each microsystem (2) comprise electromagnetic transmission means (4, 5, 8, 11).

2. Device according to claim 1, characterized in that the microsystems (2) comprise elements chosen from the group of actuators, sensors (9) and display means.

3. Device according to one of the claims 1 and 2, characterized in that the electromagnetic transmission means comprise radio frequency transmission and/or receipt means (5, 11).

4. Device according to claim 3, characterized in that the electromagnetic transmission means comprise antennas (4, 8).

5. Device according to any one of the claims 1 to 4, characterized in that, the control circuit (3) comprising power supply means (7) connected to the transmission means (4, 5) of the control circuit (3) to enable power supply of the microsystems (2) by means of their respective transmission means (4, 5, 8, 11), each microsystem (2) comprises energy recovery means (12) connected to the corresponding transmission means (11).

6. Device according to claim 5, characterized in that each microsystem (2) comprises energy storage means (12).

7. Device according to any one of the claims 1 to 6, characterized in that each microsystem (2) comprises at least one register (13), a counter (14) and

a read-only memory (15) containing an identification (code ID) of the associated microsystem (2).

8. Method of addressing the microsystems (2) of a device according to claim 7, characterized in that it comprises an initialization phase successively comprising, for each microsystem (2), addressing of the microsystem (2), by the control circuit (3), by its identification code (ID) and storing in the register (13) of the microsystem (2) of a reduced addressing code (C) supplied by the control circuit (3), each subsequent addressing phase of the microsystems (2) comprising:

- transmission, by the control circuit (3), of a reset signal (RAZ),
- transmission, by the control circuit (3), of successive increment signals (S1, S2, S3),

each microsystem (2), monitoring resetting of its counter (14) upon receipt of a reset signal (RAZ) and incrementation of the content (Sc) of its counter (14) upon receipt of an increment signal (S1), comparing the contents (Sc, C) of its counter (14) and of its register (13) so as to trigger execution of a pre-determined command when these contents (Sc, C) are identical.

9. Method of addressing according to claim 8, characterized in that the reduced addressing code (C) of a microsystem (2) is a function of its position in the array (1).

10. Method of addressing according to one of the claims 8 and 9, characterized in that the reduced addressing codes (C) of the microsystems (2) correspond to increasing numbers starting from a first microsystem.

11. Method of addressing according to any one of the claims 8 to 10, characterized in that the microsystems (2) are arranged in lines and columns, the reduced addressing code (C) of each microsystem (2) comprising a line number and a column number respectively stored in line and column

registers (13) of the microsystem (2), the contents (C) of the line and column registers (13) being respectively compared with the contents (Sc) of the line and column counters (14) of the microsystem.

12. Method of addressing according to claim 11, characterized in that the control circuit (3) successively transmits line increment signals (S1) and column increment signals (S2), the line increment signals (S1) causing the content (Sc) of the line counters (14) to be incremented and the column increment signals (S2) causing the content (Sc) of the column counters (14) to be incremented and the line counters (14) of all the microsystems (2) to be reset.

13. Method of addressing according to claim 12, characterized in that the microsystems (2) are arranged in lines, in columns and according to height, the reduced addressing code (C) comprising an additional number associated to the height, stored in an additional register (13) associated to the height, each microsystem (2) comprising an additional counter (14) associated to the height, the content (C) of the register (13) associated to the height being compared with the content (Sc) of the counter (14) associated to the height.

14. Method of addressing according to claim 13, characterized in that the control circuit (3) transmits height increment signals (S3) causing the additional counters (14) associated to the height to be incremented and the line and column counters (14) of all the microsystems (2) to be reset.

15. Method of addressing according to any one of the claims 8 to 14, characterized in that a microsystem (2) transmits an acquit signal after it has executed its command.

16. Method of addressing according to any one of the claims 8 to 15, characterized in that the control circuit (3) transmits data representative of the type of command to be executed by the microsystems (2) in association with transmission of a reset signal (RAZ).

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17. Method of addressing according to any one of the claims 8 to 16, characterized in that the control circuit (3) transmits data representative of the type of command to be executed by the microsystems (2) in association with transmission of an increment signal (S1, S2, S3).

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